applying the event based test vectors to the device model and evaluating the response output of the device model;

modifying the event based test vectors by the event test system to acquire desired response outputs from the device model;

feedbacking the modified event based test vectors to the EDA tools to modify the design data, thereby correcting design errors in the design data.

REMARKS

This preliminary amendment is submitted for claiming the benefit of the provisional application and correct minor errors in the specification and claims. No new matter has been introduced by this amendment.

Applicant respectfully requests the entrance of the amendment before substantive examination of the instant case.

Respectfully submitted,

MURAMATSU & ASSOCIATES

Dated: 11/14/2001

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

(1) The following paragraph has been inserted between line 1 and line 2 in Page 1:

This application claims the benefit of Provisional Patent Application No. 60/237,001 filed September 29, 2000.

(2) The paragraph from page 16, line 21 to page 16, line 30 has been replaced with the following:

The event based test system (design test station DTS) 82 includes a VCD compiler 218, an event viewer 222, and a VCD writer 220. The VCD compiler 218 translates the VCD data to event data for use by the event based test system 82. The event viewer 222 and the VCD writer 220 correspond to the VCD waveform viewer/editor 87 and event waveform editor/viewer 88 in Figure 5 to monitor and modify the event based test vectors. A scheduler 216 is provided to monitor and manage tasks and communication between the event test system 82 and the simulator 190.

IN THE CLAIMS:

Claims 12-20 have been amended as follows:

[12] 11. (Amended) A method of validating design of complex integrated circuits as defined in Claim 10, wherein said device model is either dependent of a particular simulator or independent of any simulator.

[13] 12. (Amended) A method of validating design of complex integrated circuits as defined in Claim 10, further comprising a step of linking EDA tools including a simulator with the event based test system through a software interface.

[14] 13. (Amended) A method of validating design of complex integrated circuits as defined in Claim 10, further comprising a step of extracting event format data through a testbench produced in the IC design data.

[15] 14. (Amended) A method of validating design of complex integrated circuits as defined in Claim **[14]** 13, wherein said step of extracting the event format data including a step of executing the testbench by the simulator and extracting the event format data from a value change dump file produced by the simulator.

[16] 15. (Amended) A method of validating design of complex integrated circuits as defined in Claim **[14]** 13, further comprising a step of installing the extracted event data in the event test system and generating event based test vectors using the extracted event data by the event based test system to apply the event based test vectors to the device model.

[17] 16. (Amended) A method of validating design of complex integrated circuits as defined in Claim 10, further comprising a step of creating a new testbench based on the modified event based test vectors from the event based test system.

[18] 17. (Amended) A method of validating design of complex integrated circuits as defined in Claim 10, said EDA tools

including means for viewing and editing waveforms derived from the testbench created in the IC design data.

[19] 18. (Amended) A method of validating design of complex integrated circuits as defined in Claim 10, said event based test system including means for viewing and editing waveforms of event based test vectors extracted from a testbench created in the IC design data and means for changing clock rate and event timing data of the event based test vectors applied to the device model.

[20] 19. (Amended) A method of validating design of complex integrated circuits (IC) where a design process is carried out under electronic design automation (EDA) environment, comprising the following steps of:

preparing a device model of an IC to be designed based on IC design data produced under the EDA environment;

linking EDA tools including a simulator with an event based test system;

extracting event format data from data file resulted from executing a testbench produced in the IC design data by the simulator;

installing the extracted event data in the event test system and generating event based test vectors using the event data by the event based test system;

applying the event based test vectors to the device model and evaluating the response output of the device model;

modifying the event based test vectors by the event test system to acquire desired response outputs from the device model;

feedbacking the modified event based test vectors to the EDA tools to modify the design data, thereby correcting design errors in the design data.